

Machine Cycle	Status			Control Signals		
	$\overline{\text{IO/M}}$	S1	S0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INTA}}$
Opcode Fetch	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read	1	1	0	0	1	1
I/O Write	1	0	1	1	0	1
Interrupt Acknowledge	1	1	1	1	1	0
HALT	Z	0	0	Z	Z	1
HOLD	Z	X	X	Z	Z	1
RESET	Z	X	X	Z	Z	1

Where Z is tri state (pin neither connected to supply nor ground. High impedance) and X represents do not care.

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8085 Instruction Set With Machine Cycle

Chao Zhang



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